REMARKS

In the Office Action mailed June 23, 2006, claims 1 and 23 are objected to as being inconsistent with the remaining claims. Applicants have amended each of the independent claims 1 and 23 to include the abbreviation DFS for the digital frequency synthesizer as suggested by the Examiner. Claims 5-7 are also rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended claim 5 to correctly depend from claim 1 rather than claim 4 which had been cancelled. Applicants respectfully submit that claims 5-7 are now in proper form.

Claims 1-2, 5, 9, 12-13, 18 and 23 are rejected under 35 USC §103(a) as being unpatentable over Agarwal et. al. (U.S. Patent 6,633,288, "Agarwal") in view of Yoon et al. (U.S. Patent 6,445,234, "Yoon") and Ragan et al. (U.S. Patent 6,188,288, "Ragan"). Claims 3, 10, 11 and 14-17 are objected to as being dependent upon a rejected base claim, but would be allowed if put in independent form including all of the limitations of the base claim and any intervening claims.

In response to the rejection of the claims, Applicants have amended independent claim 3 to include the limitations of claim 1. Applicants submit that claim 3 is now in allowable form. Applicants have also amended claim 14 to include all of the limitations of the pending claim 1 and to put claim 14 in allowable form. Applicants respectfully submit that claim 14 as amended and dependent claims 15-17 are also in allowable form.

Applicants have also amended claim 1 to overcome the rejection. In particular, Applicants have amended claim 1 to indicate that the digital frequency synthesizer is coupled to receive a clock signal generated by the delay lock loop. Applicants respectfully submit that claim 1 as amended clearly distinguish over the combination of references. The primary reference Agarwal relates to a circuit for optimizing graphic images from video signals. The basic principle of Agarwal is to iteratively find the phase and frequency for which the image quality is the highest. (Col. 3, lines 23-42). It is suggested in the Office Action that elements 406 and 416 of Agarwal disclose a

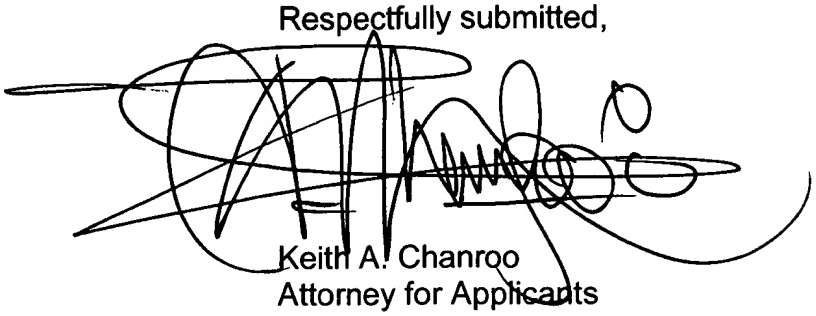
frequency synthesizer. However, each of the independent claims 1 and 23 includes a digital frequency synthesizer coupled to receive a clock signal generated by the delay lock loop. In particular, claim 1 as amended comprises a digital frequency synthesizer coupled to receive the output of a delay lock loop. Similarly, claim 23 comprises a digital frequency synthesizer coupled to the delay lock loop, wherein the delay lock loop drives a synchronizing clock signal to the digital frequency synthesizer. While Agarwal discloses an analog video interface having a PLL and a DLL to generate signals having different phases and frequencies, there is no teaching or suggestion in Agarwal of a digital frequency synthesizer as claimed. That is, the frequency synthesizer of Agarwal receives an analog HSYNC TV signal. The optimized output of the computation unit 408 of Agarwal is coupled to a digitizer 402 to generate a digital TV signal. Further, there is no teaching or suggestion in Agarwal of a digital frequency synthesizer receiving the output of a delay lock loop. In contrast, the only output of the delay lock loop of Agarwal is provided to a computation unit 408, which measures signal quality and enables the selection of a phase and delay for the signal which provides the best signal quality. While Yoon and Ragan are cited for disclosing specific inputs of a delay lock loop or digital frequency synthesizer, neither reference discloses or suggests a digital frequency synthesizer coupled to receive a clock signal generated by the delay lock loop as claimed in each of claims 1 and 23. Applicants respectfully submit that the combination of references fails to disclose or suggest Applicants' claim 1 as amended or claim 23, and respectfully request reconsideration of the rejection.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-7710.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 31, 2006.

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